



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **OSHIMA, Tadashi**

Group Art Unit: **2814**

Serial No.: **09/996,758**

Examiner: **PHAM, Hoai V.**

Filed: **November 30, 2001**

P.T.O. Confirmation No.: **4892**

For: **SEMICONDUCTOR DEVICE WITH TWO TYPES OF FET'S HAVING DIFFERENT GATE LENGTHS AND ITS MANUFACTURE METHOD**

AMENDMENT TRANSMITTAL

Commissioner for Patents
Washington, D.C. 20231

April 7, 2003

Sir:

Transmitted herewith is an Amendment in the above-identified application.
The fee has been calculated as shown below:

	CLAIMS AS AMENDED						
	Claims Remaining After Amendment	Highest Number Previously Paid For		Present Extra	Small Entity	Large Entity	Additional Fee
Total Claims	11	20	=		X \$9	X \$18	
Independent Claims	5	4	=	1	X \$42	X \$84	84.00
First Presentation of Multiple Dependent Claims					\$140	280	
TOTAL FEES ENCLOSED:							\$ 84.00

XX Enclosed please find our check in the amount of \$ 84.00 for the additional claims fee in connection with this amendment.

XX The Commissioner is hereby authorized to charge payment for any additional fees associated with this communication or credit any overpayment to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP

Sadao Kinashi

Sadao Kinashi
Attorney for Applicant
Reg. No. 48,075

SK/fs
Atty. Docket No. **011318**
Suite 1000
1725 K Street, N.W.
Washington, D.C. 20006
(202) 659-2930



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THE UNITED STATES PATENT AND TRADEMARK OFFICE

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OSHIMA, Tadashi

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P.T.O. Confirmation No.: 4892

For: **SEMICONDUCTOR DEVICE WITH TWO TYPES OF FET'S HAVING DIFFERENT GATE LENGTHS AND ITS MANUFACTURE METHOD**

AMENDMENT UNDER 37 CFR §1.111

Commissioner for Patents
Washington, D.C. 20231

April 7, 2003

Sir:

In response to the Office Action dated January 7, 2003, please amend the above-identified application as follows:

IN THE CLAIMS:

Please **AMEND** the claims as follows:

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4. (Amended) A semiconductor device comprising:

A¹
a first field effect transistor having a first gate electrode formed on a first section of a semiconductor substrate;

a second field effect transistor having a second gate electrode formed on the second section of said semiconductor substrate; and